What is claimed is:

1. An architecture for reading microprocessor's instructions, comprising:

a processing unit for executing arithmetic logic operation, controlling, and pre-reading the instruction(s) next to the current one;

an instruction buffer register for reading instruction addresses;

a program memory module for storing instructions; and

an instruction reading-amount register for setting the amount of instructions to be read;

whereby, in the instruction processing procedure, the processing unit is supposed to pre-read an instruction next to the current one for setting the state of the instruction reading-amount register, wherein, in the case the next instruction is decoded and found a conditional branch one, the instruction reading-amount register is set in a state for reading two instructions such that, in the next instruction cycle, one of those two instructions will be determined according to the processing unit and read by the instruction buffer register; or, in the case the next instruction is found an instruction other than the conditional branch one, the instruction reading-amount register is set in a state for reading an instruction only, such that the instruction buffer register will read an instruction in a succeeding instruction cycle to thereby waive unnecessary reading of the program memory for reducing power consumption.

2. The architecture according to claim 1, wherein, in the case the next instruction is a normal state arithmetic logic instruction, 1 is added to the address of the program counter (PC) for reading a following instruction; or, in the case the next instruction is an unconditional branch one, an instruction at a new address will be read in the next instruction cycle; or, in the case the next instruction is a

"CALL" or a "RETURN" instruction, an instruction at a new address or in the "STACK" will be read in the next instruction cycle.

3. The architecture according to claim 1, wherein a binary "1" or "0" is set in the instruction reading-amount register to represent the state for reading two instructions or one.

4. An architecture for reading microprocessor's instructions, comprising:

an instruction reading-amount register for setting the amount of instructions to be read;

a processing unit for executing arithmetic logic operation, controlling, and pre-reading the instruction(s) next to the current one;

an instruction buffer register for reading instruction addresses;

a program memory module composed of an odd-page and an even-page program memory portion for storing instructions;

an address buffer register composed of an odd and an even address buffer register for storage of an odd or an even instruction address selected by a corresponding multiplexer;

an incremental circuit for adding 1 to an instruction address of the address line set;

a first multiplexer for choosing the odd instruction addresses;

a second multiplexer for choosing the even instruction addresses;

a third multiplexer for choosing an instruction address in the odd-page or the even-page program memory portion;

a fourth multiplexer for enabling the even address buffer register for reading an instruction address of the even-page program memory portion;

a fifth multiplexer for enabling the odd address buffer register for reading

an instruction address of the odd-page program memory portion;

a sixth multiplexer for controlling the third multiplexer to choose an instruction address in the odd-page or the even-page program memory portion;

whereby the processing unit will pre-read and pre-decode a next instruction for setting the state of the instruction reading-amount register, which, suppose the pre-decoded instruction is found a conditional branch one, would be set in a state for reading two instructions such that, in a next instruction cycle, the next two instruction addresses in the odd or even address buffer register are read, which are then decoded by the processing unit and selected for execution in order via the sixth multiplexer; or in the event the pre-decoded instruction is found an instruction other than the conditional branch one, then the instruction reading-amount register is set for reading a single instruction only, such that, in a next instruction cycle, an instruction address in the odd or even address buffer register would be fetched for execution in order to save the breath of reading any unnecessary program memory to thereby reduce power consumption accordingly.

5. The architecture according to claim 4, in which, if the pre-read and pre-decoded instruction is found a general arithmetic logic instruction, an instruction in the program memory at address PC+1 will be fetched in a next instruction cycle; or, if the pre-read and pre-decoded instruction is found an unconditional branch one, an instruction in the program memory at a new address pointed by the branch one will be fetched in the next instruction cycle; or, if the pre-read and pre-decoded instruction is found a "CALL" or a "RETURN" instruction, an instruction in the program memory at a new address pointed by the "CALL" instruction will be fetched, or an instruction according to a return address on the "STACK" will be read and fetched.

6. The architecture according to claim 4, wherein the instruction reading-amount register is set "1" or "0" to represent reading two instructions or one respectively.